What is claimed is:

1. An insulated gate bipolar transistor comprising:

a first semiconductor layer of a first conductivity type;

a second semiconductor layer of a second conductivity type formed on a top surface of said first semiconductor layer;

a base layer of the first conductivity type formed on a top surface of said second semiconductor layer;

a plurality of gate electrodes each of which is buried in a trench with a gate insulation film interposed therebetween, said trench being formed in said base layer to a depth reaching said second semiconductor layer from a surface of said base layer, each said gate electrode having an upper surface of a rectangular pattern with different widths in two orthogonal directions, said gate electrodes being disposed in a direction along a short side of the rectangular pattern;

emitter layers of the second conductivity type formed in the surface of said base layer to oppose both end portions of each said gate electrode in a direction along a long side of the rectangular pattern;

a first main electrode in contact with said emitter layers and said base layer; and

a second main electrode formed at a bottom surface of said first semiconductor layer.

2. The transistor according to claim 1, wherein said

emitter layers are formed as impurity diffusion layers opposing three side faces at the both end portions of each said gate electrodes in the long side direction.

3. The transistor according to claim 2, wherein said emitter layers are impurity diffusion layers formed independently of each other at the both end portions of each said gate electrode in the long side direction.

4. The transistor according to claim 2, wherein said emitter layers are impurity diffusion layers continuously formed to extend ~~and~~ overlie said plurality of gate electrodes while opposing the both end portions of each said gate electrode in the long side direction.

5. The transistor according to claim 2, wherein said gate electrodes include multiple ones aligned in the long side direction also, and wherein said emitter layers are impurity diffusion layers formed to continue between two neighboring gate electrodes while opposing respective end portions of said two neighboring gate electrodes in the long side direction.

6. The transistor according to claim 2, further comprising:

a coupling portion configured to connect said plurality of gate electrodes together at their central portions in the long side direction, said coupling portion being the same in structure as said gate electrodes.

7. The transistor according to claim 6, wherein said emitter layers are impurity diffusion layers formed

independently of each other at the both end portions of each said gate electrode in the long side direction.

8. The transistor according to claim 6, wherein said emitter layers are impurity diffusion layers continuously formed to extend ~~and overlie~~ said plurality of gate electrodes while opposing the both end portions of each said gate electrode in the long side direction.

9. The transistor according to claim 6, wherein said gate electrodes include multiple ones aligned in the long side direction also and wherein said emitter layers are impurity diffusion layers formed to continue between two neighboring gate electrodes while opposing respective end portions of said two neighboring gate electrodes in the long side direction.

10. The transistor according to claim 1, further comprising:

a coupling portion configured to connect said plurality of gate electrodes together at their both end portions in the long side direction, said coupling portion being the same in structure as the gate electrodes.

11. The transistor according to claim 10, wherein said emitter layers are impurity diffusion layers formed independently of each other at the both end portions of each said gate electrode in the long side direction.

12. The transistor according to claim 10, wherein said emitter layers are impurity diffusion layers formed to continue along said coupling portion while opposing the

both end portions of each said gate electrode in the long side direction.

13. The transistor according to claim 10, wherein said gate electrodes include multiple ones aligned in the long side direction also and wherein said emitter layers are impurity diffusion layers formed to continue between two neighboring gate electrodes while opposing respective end portions of said two neighboring gate electrodes in the long side direction.